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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,613	09/16/2003	Mehrdad Mahanpour	H0947	3552

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,613	MAHANPOUR, MEHRDAD	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/663613 file on 09/16/03.

Claim 1-8 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Mok et al. (US Patent 6791171).

3. As to claims 1, Mok et al. teach a method for testing the design comprising the steps of: (a) desiring the system IC to have a predetermined number and pattern for its chip I/0 pads (see fig 1-4 and col 14 lines 57 to col 15 line 45); (b) designing a packaging module to fan-out the I/0 of the system IC to an expanded pitch of packaging I/0 pads having a correspondence to said chip I/0 pads (see fig 15-17 col 18 lines 15 to col 19 lines 9); (c) partitioning circuitry of said system IC into a functional circuit (see fig 16-21 col 18 lines 36 to col 20 lines 24); (d) desiring said functional circuit as a corresponding test IC, wherein said test IC I/0 pads conform to one of a sub-set of the number and pattern of said chip of an integrated circuit (system IC) I/0 pads (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21); (e) attaching said test IC to said packaging module with conductive material (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21); f) exercising said test IC by applying signals and power to inputs of said packaging module at

packaging I/0 pads corresponding to said sub-set of chip I/0 pads (see fig 75, 76 col 36 lines 20 to col 37 lines 21); and (g) collecting test data corresponding to said test IC (see fig 75, 76 col 36 lines 20 to col 37 lines 21).

4. As to claims 2, Mok et al. teach a method for testing the design of an integrated circuit (system IC) composing the steps of: (a) designing said system IC to have a predetermined number and pattern for its chip I/0 pads pads (see fig 1-4 and col 14 lines 57 to col 15 line 45); (b) designing a packaging module to fan-out the chip I/0 to an expanded pitch of packaging I/0 pads having a correspondence to said chip 1/0 pads (see fig 15-17 col 18 lines 15 to col 19 lines 9); (c) partitioning functionality of said system IC into a plurality of individual functional circuits (see fig 16-21 col 18 lines 36 to col 20 lines 24); (d) desiring said plurality of individual functional circuits as a corresponding plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of sub-sets of chip I/O pads making up said number and pattern of said chip I/O pads (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21); (e) attaching said plurality of test 1Cs to said packaging module with conductive material (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21); f) interconnecting an I/0 of a first test IC of said plurality of test ICs to an I/O of a second test IC of said plurality of test ICs extemal to said packaging module (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21); (g) operating said plurality of test ICs by applying signals and power to selected ones of said packaging I/0 pads corresponding to said plurality of sub-sets of said number and pattern of said chip I/0 pads (see fig 75, 76 col 36 lines 20 to col 37 lines 21); and (h) collecting test data corresponding to operating said plurality of test Ics (see fig 75, 76 col 36 lines 20 to col 37 lines 21).

5. As to claims 3, Mok et al. teach further comprising the steps of: redesigning a first test IC of said plurality of test 1Cs generating a redesigned first test IC in response to said test data; replacing a corresponding one of said plurality of tests chips with said redesigned first test IC; and repeating steps (e)-(g) (see fig 54, 55 75, 76 col 34 lines 65 to col 37 lines 21).

6. As to claims 4, Mok et al. teach further comprising the step of: redesigning said functionality of said system IC in response to said test data (see fig 75, 76 col 36 lines 20 to col 37 lines 21 and background).

7. As to claims 5, Mok et al. teach further comprising the steps of: coupling said system IC onto a PCB for a system designed to use said system IC (see fig 76-78 col 36 lines 20 to col 38 lines 37); and operating said system IC to emulate at least one function of said system (see fig 76-78 col 36 lines 20 to col 38 lines 37).

8. As to claims 6, Mok et al. teach further comprising the step of: testing said system IC in a test fixture desired for said system IC (see fig 76-78 col 36 lines 20 to col 38 lines 37 and summary)

9. As to claims 7, and 8 Mok et al. teach a test module for a production system IC having a particular number and pattern of chip I/0 pads, comprising: a test IC corresponding to a sub-set of a total functionality of said system IC, said test IC having a test IC I/0 configuration corresponding to a sub-set of said particular number and pattern of chip I/0 pads pads (see fig 1-4 and col 14 lines 57 to col 15 line 45); a packaging module designed for said production system IC, having a packaging I/0 number and pattern of packaging I/0 pads for receiving said particular number and pattern of chip 1/0 pads (see fig 15-17 col 18 lines 15 to col 19 lines 9); couplings for electrically coupling said test IC I/0 configuration to selected ones of said packaging I/0 pads

corresponding to said sub-set of said particular number and pattern of chip I/0 pads (see fig 54, 55, 75, 76 col 34 lines 65 to col 37 lines 21); and couplings for electrically coupling test signals to said selected ones of said packaging 1/0 pads corresponding to said sub-set of said particular number and pattern of chip I/0 pads (see fig 54, 55, 75-78 col 34 lines 65 to col 38 lines 21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on 571 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
November 12, 2005

THUAN D.D
Primary examiner.
11/14/05.